LOW VOLTAGE DUAL ½-H-BRIDGE DRIVER IC

Check for Samples: DRV8839

FEATURES

- **Dual ½-H-Bridge Motor Driver**
  - **Drives a DC Motor or One Winding of a Stepper Motor, or Other Loads**
  - **Low MOSFET On-Resistance: HS + LS 280 mΩ**
- **1.8-A Maximum Drive Current**
- **Separate Motor and Logic Supply Pins:**
  - **0-V to 11-V Motor-Operating Supply-Voltage Range**
  - **1.8-V to 7-V Logic Supply-Voltage Range**
- **Separate Motor and Logic Supply Pins**
- **Individual ½-H-Bridge Control Input Interface**
- **Low-Power Sleep Mode With 120-nA Maximum Combined Supply Current**
- **2-mm x 3-mm 12-Pin WSON Package**

APPLICATIONS

- **Battery-Powered:**
  - **DSLR Lenses**
  - **Consumer Products**
  - **Toys**
  - **Robotics**
  - **Cameras**
  - **Medical Devices**

DESCRIPTION

The DRV8839 provides a versatile power driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered applications. The device has two independent ½-H-bridge drivers and can drive one DC motor or one winding of a stepper motor, as well as other devices like solenoids. The output stages use N-channel power MOSFET's configured as ½-H-bridges. An internal charge pump generates needed gate drive voltages.

The DRV8839 can supply up to 1.8-A of output current. It operates on a motor power supply voltage from 0 V to 11 V and a device power supply voltage of 1.8 V to 7 V.

The DRV8839 has independent input and enable pins for each ½-H-bridge which allow independent control of each output.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature.

The DRV8839 is packaged in a 12-pin, 2-mm x 3-mm WSON package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

ORDERING INFORMATION(1)

PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
PowerPAD™ (WSON) - DSS	Reel of 3000	DRV8839DSSR	8839

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM

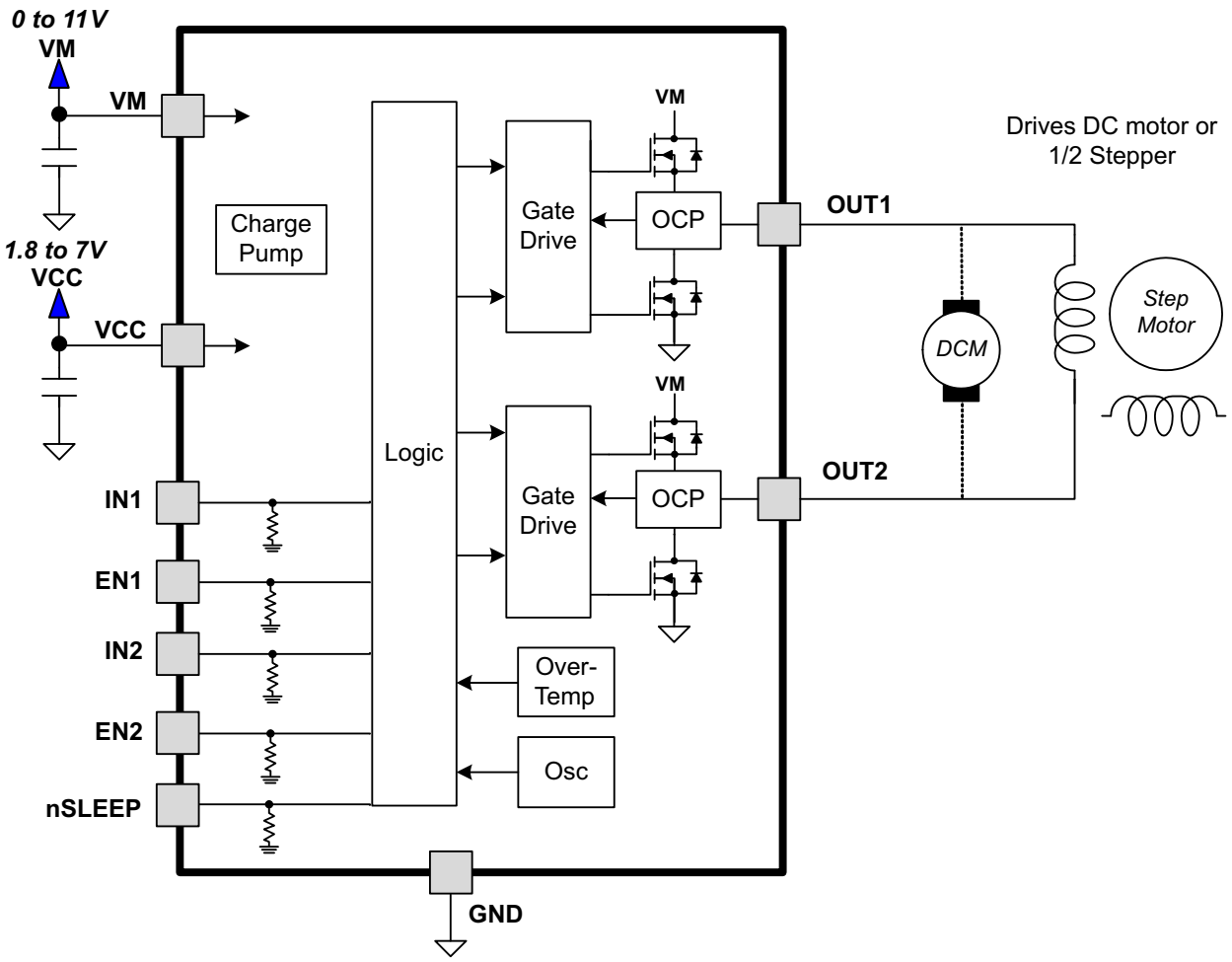
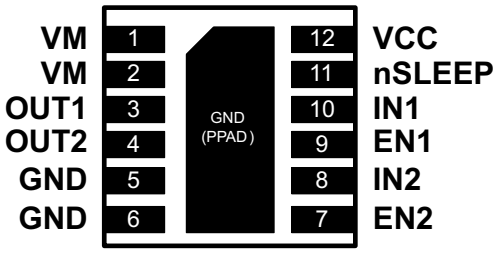


Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	5, 6	-	Device ground	
VM	1, 2	-	Motor supply	Bypass to GND with a 0.1-µF, 16-V ceramic capacitor.
VCC	12	-	Device supply	Bypass to GND with a 0.1-µF, 6.3-V ceramic capacitor.
CONTROL				
nSLEEP	11	I	Sleep mode input	Logic low puts device in low-power sleep mode Logic high for normal operation Internal pulldown resistor
IN1	10	I	Input 1	Logic input controls OUT1 Internal pulldown resistor
EN1	9	I	Enable 1	Logic high enables OUT1 Internal pulldown resistor
IN2	8	I	Input 2	Logic input controls OUT2 Internal pulldown resistor
EN2	7	I	Enable 2	Logic high enables OUT2 Internal pulldown resistor
OUTPUT				
OUT1	3	O	Output 1	Connect to motor winding
OUT2	4	O	Output 2	
NO CONNECT				
NC	2, 5	-	No connection	No connection to these pins

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

DSS PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS(1)(2)

		VALUE	UNIT
VM	Power supply voltage range	-0.3 to 12	V
VCC	Power supply voltage range	-0.3 to 7	V
	Digital input pin voltage range	-0.5 to 7	V
	Peak motor drive output current	Internally limited	A
T_J	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8839 DSS 12 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	50.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	58	
θ_{JB}	Junction-to-board thermal resistance(4)	19.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.9	
ψ_{JB}	Junction-to-board characterization parameter(6)	20	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	6.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

T_A = 25°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Device power supply voltage range	1.8		7	V
V_M	Motor power supply voltage range	0		11	V
I_{OUT}	H-bridge output current(1)	0		1.8	A
f_{PWM}	Externally applied PWM frequency	0		250	kHz
V_{IN}	Logic level input voltage	0		5.5	V

(1) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V (unless otherwise noted)

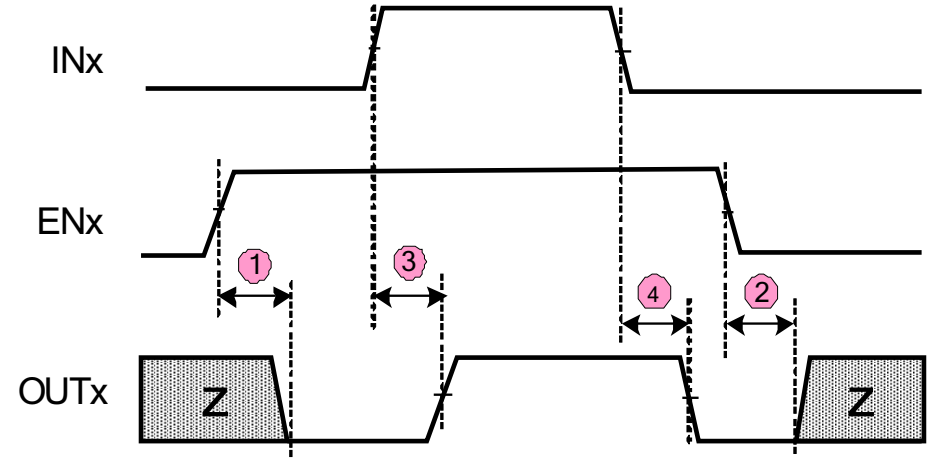
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{VM}	VM operating supply current	No PWM		40	100	µA
		50 kHz PWM		0.8	1.5	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0 V		30	95	nA
I_{VCC}	VCC operating supply current	No PWM		300	500	µA
		50 kHz PWM		0.7	1.5	mA
I_{CCQ}	VCC sleep mode supply current	nSLEEP = 0 V		5	25	nA
V_{UVLO}	VCC undervoltage lockout voltage	V_{CC} rising			1.8	V
		V_{CC} falling			1.7	
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage		0.31 x V_{CC}	0.34 x V_{CC}		V
V_{IH}	Input high voltage			0.39 x V_{CC}	0.43 x V_{CC}	V
V_{HYS}	Input hysteresis			0.08 x V_{CC}		V
I_{IL}	Input low current	V_{IN} = 0	-5		5	µA
I_{IH}	Input high current	V_{IN} = 3.3 V			50	µA
R_{PD}	Pulldown resistance			100		kΩ
H-BRIDGE FETS						
$R_{DS(ON)}$	HS + LS FET on resistance	I_O = 800 mA, T_J = 25°C		280	330	mΩ
I_{OFF}	Off-state leakage current				±200	nA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		1.9		3.5	A
t_{OCR}	Overcurrent protection retry time			1		ms
t_{DEAD}	Output dead time			100		ns
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

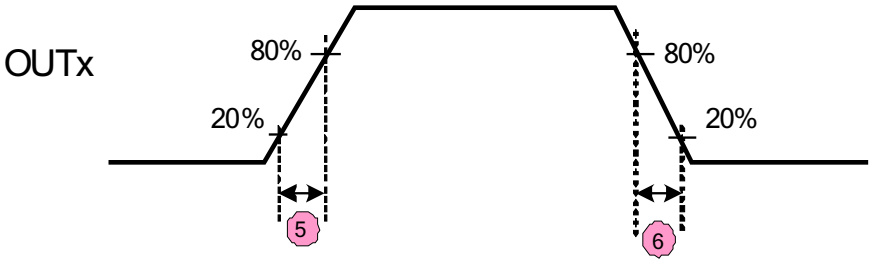
TIMING REQUIREMENTS(1)

T_A = 25°C, V_M = 5 V, V_{CC} = 3 V, R_L = 20 Ω

NO.	PARAMETER	CONDITIONS	MIN	MAX	UNIT
1	t_1	Output enable time		120	ns
2	t_2	Output disable time		120	ns
3	t_3	Delay time, INx high to OUTx high		120	ns
4	t_4	Delay time, INx low to OUTx low		120	ns
5	t_5	Output rise time	50	150	ns
6	t_6	Output fall time	50	150	ns

(1) Not production tested – ensured by design





FUNCTIONAL DESCRIPTION

Bridge Control

The DRV8839 is controlled using separate enable and input pins for each ½-H-bridge.

The following table shows the logic for the DRV8839:

ENx	INx	OUTx
0	X	Z
1	0	L
1	1	H

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the DRV8839 will enter a low-power sleep mode. In this state all unnecessary internal circuitry is powered down.

Power Supplies and Input Pins

The input pins may be driven within their recommended operating conditions with or without the VCC and VM power supplies present. No leakage current path will exist to the supply. There is a weak pulldown resistor (approximately 100 kΩ) to ground on each input pin.

VCC and VM may be applied and removed in any order. When VCC is removed, the device will enter a low power state and draw very little current from VM. If the supply voltage is between 1.8 V and 7 V, VCC and VM may be connected together.

The VM voltage supply does not have any undervoltage lockout protection (UVLO), so as long as VCC > 1.8 V, the internal device logic will remain active. This means that the VM pin voltage may drop to 0 V, however, the load may not be sufficiently driven at low VM voltages.

Protection Circuits

The DRV8839 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled. After approximately 1 ms, the bridge will be re-enabled automatically.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all circuitry in the device is disabled and internal logic is reset. Operation resumes when VCC rises above the UVLO threshold.

APPLICATIONS INFORMATION

Motor Connections

If a single DC motor is connected to the DRV8839, it is connected between the OUT1 and OUT2 pins as shown below:

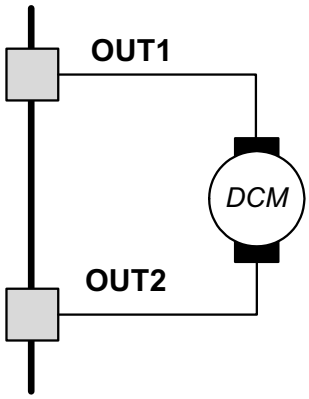


Figure 1. Single DC Motor Connection

Motor operation is controlled as follows:

EN1	EN2	IN1	IN2	OUT1	OUT2	MOTOR OPERATION
0	X	X	X	Z	See (1)	Off (coast)
X	0	X	X	See (2)	Z	Off (coast)
1	1	0	0	L	L	Brake
1	1	0	1	L	H	Reverse
1	1	1	0	H	L	Forward
1	1	1	1	H	H	Brake

(1) State depends on EN2 and IN2, but does not affect motor operation because OUT1 is tri-stated.
(2) State depends on EN1 and IN1, but does not affect motor operation because OUT2 is tri-stated.

Two DC motors may be connected to the DRV8839. In this mode, it is not possible to reverse the direction of the motors; they will turn only in one direction. The connections are shown below:

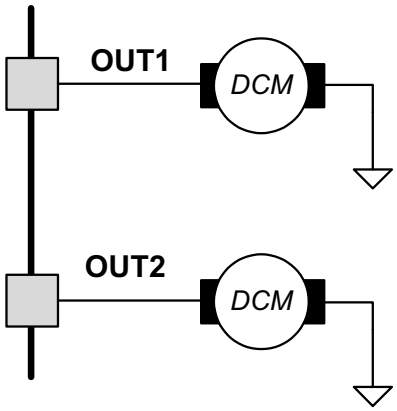


Figure 2. Dual DC Motor Connection

Motor operation is controlled as follows:

ENx	INx	OUTx	MOTOR OPERATION
0	X	Z	Off (coast)
1	0	L	Brake
1	1	H	Forward

THERMAL INFORMATION

Thermal Protection

The DRV8839 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8839 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = R_{DS(ON)} \times (I_{OUT(RMS)})^2 \quad (1)$$

Where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of the HS plus LS FETs, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases.

REVISION HISTORY

Changes from Original (January 2013) to Revision A **Page**

- Changed FEATURES bullet 1
- Changed motor supply voltage range in DESCRIPTION section 1
- Changed Motor power supply voltage range in RECOMMENDED OPERATING CONDITIONS 4
- Added t_{OCR} and t_{DEAD} parameters to ELECTRICAL CHARACTERISTICS 5
- Added paragraph to Power Supplies and Input Pins section 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8839DSSR	ACTIVE	WSON	DSS	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	8839	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

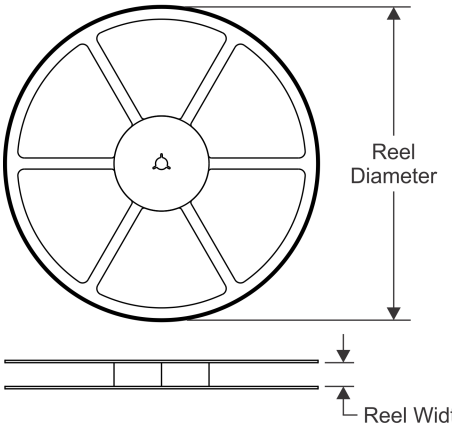
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

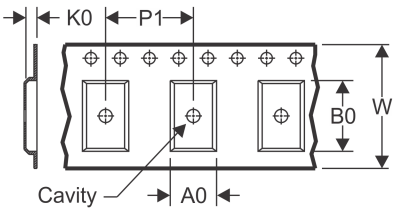
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

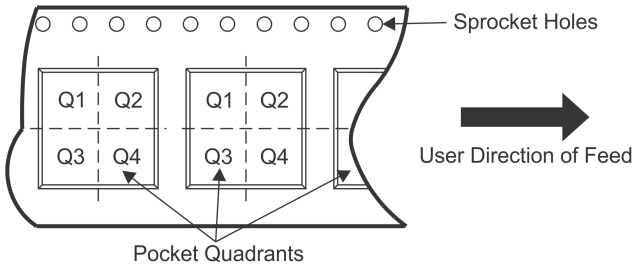


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

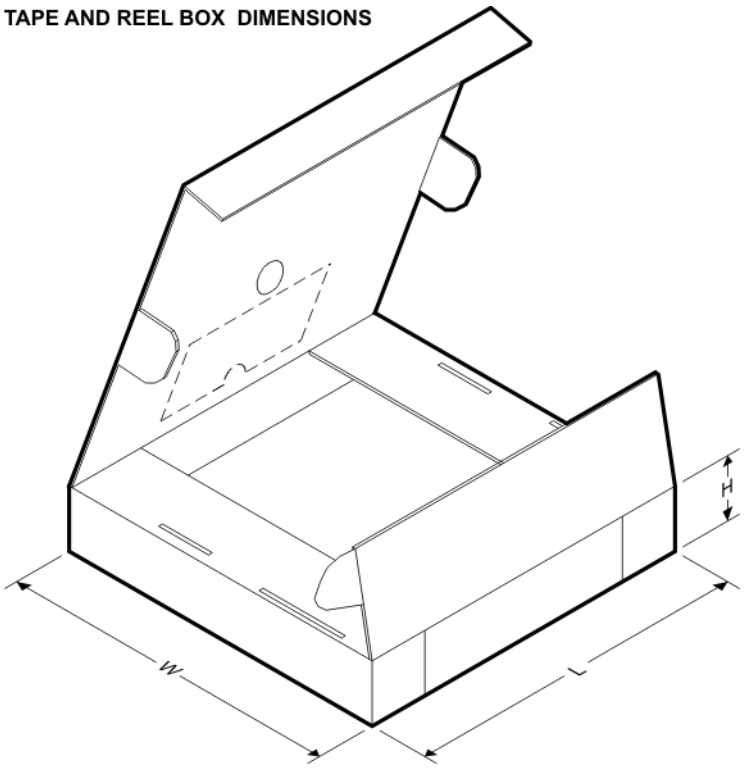
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8839DSSR	WSON	DSS	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

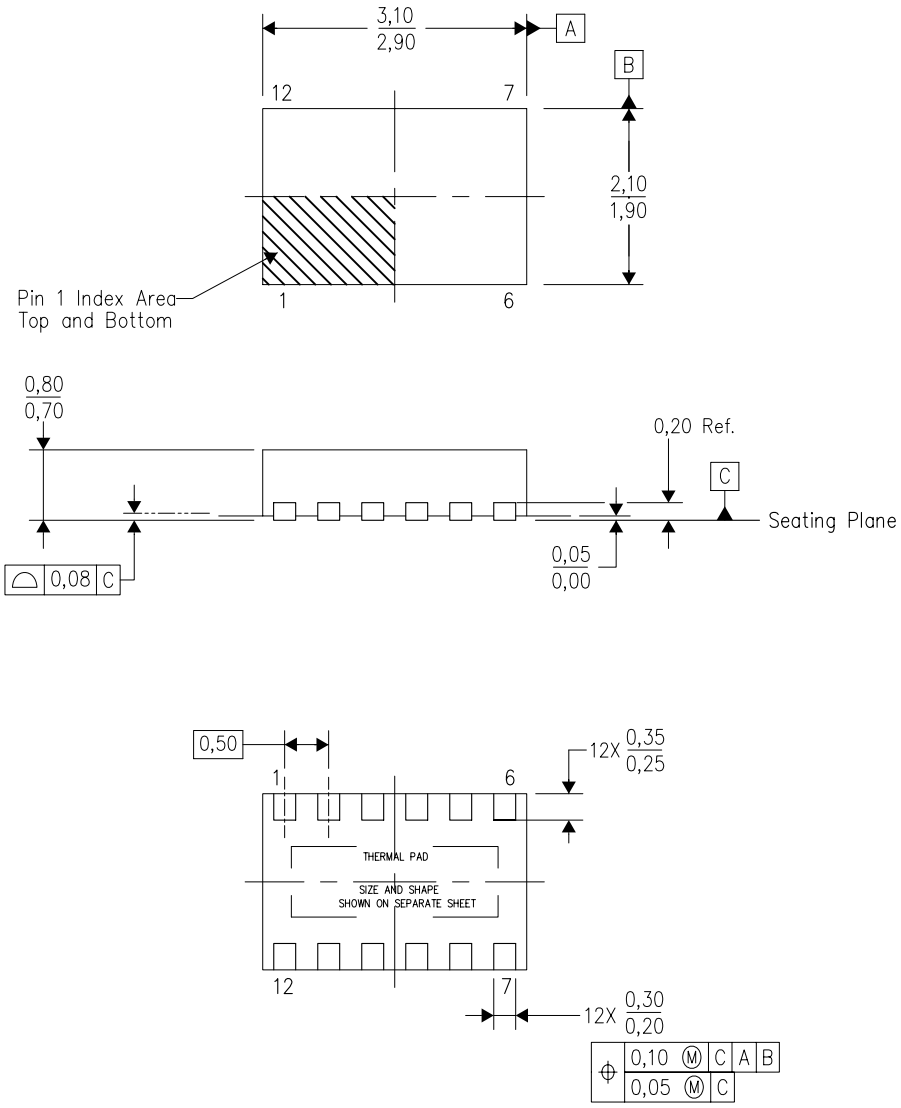
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8839DSSR	WSON	DSS	12	3000	210.0	185.0	35.0

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



4209244/C 07/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

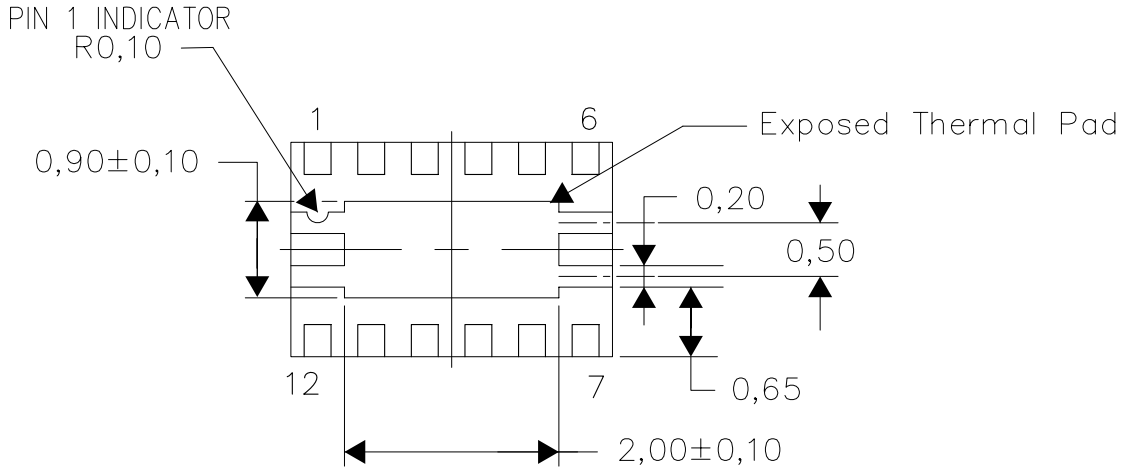
DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



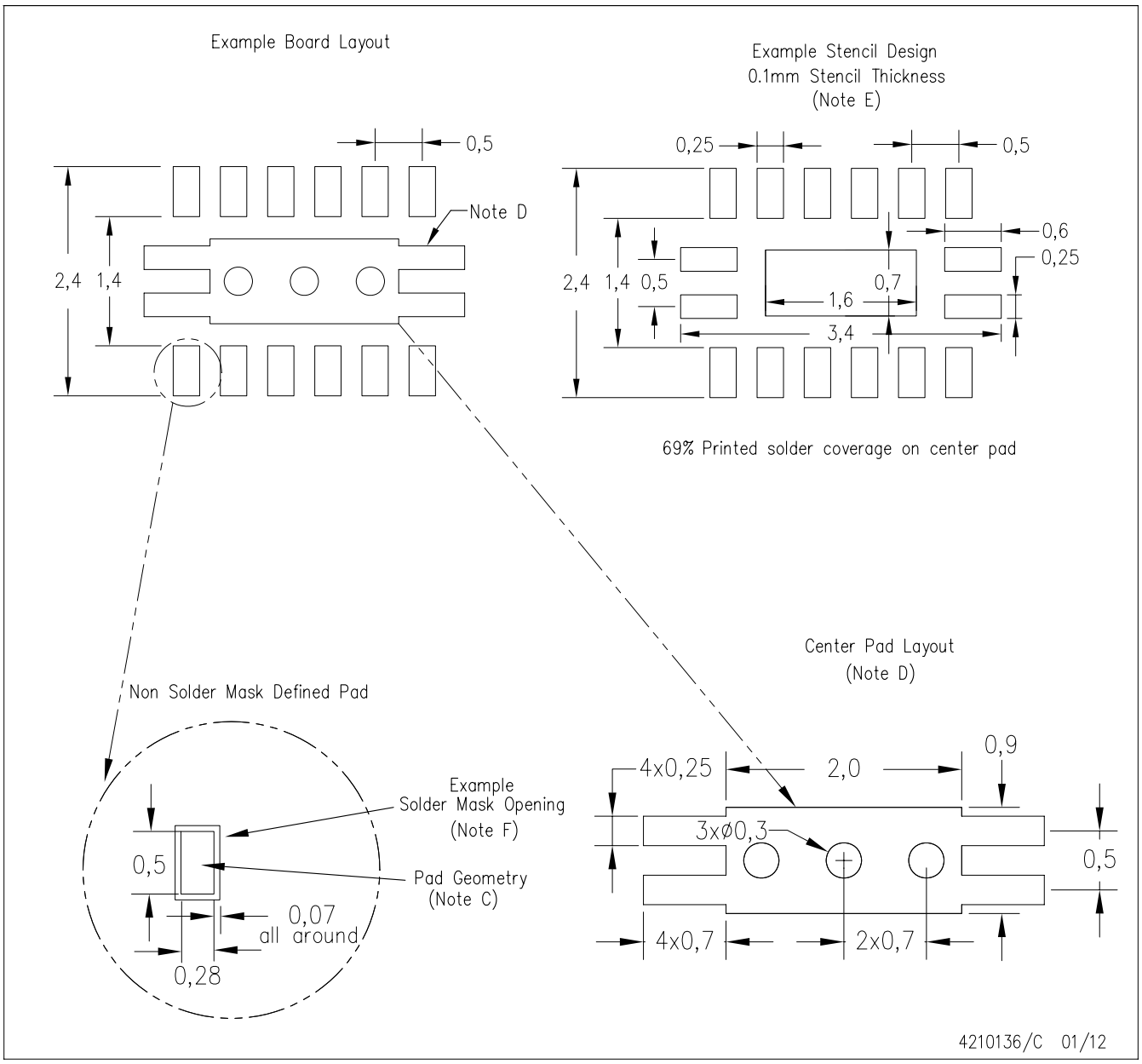
Bottom View

Exposed Thermal Pad Dimensions

4210135–2/C 02/12

NOTE: All linear dimensions are in millimeters

DSS (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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